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| EXAMINER | |
|---|---|
| FORD, KENISHA V | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/593,141 | MEINHARDT ET AL. | |
| | Examiner | Art Unit | |
| | KENISHA V. FORD | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/18/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the Application filed 18 September 2006. The Preliminary Amendment has been acknowledged. Currently, claims 16-29 are pending. Claims 1-15 have been cancelled.

### *Information Disclosure Statement*

1. The information disclosure statement (IDS) submitted on 9/18/06 is being considered by the examiner.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 16-21, 23, 24, 26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Johansson et al. (US 6,440,810 B1).

Regarding claim **16**, Johansson et al. discloses a method for the production of a bipolar transistor comprising a highly doped extrinsic base, wherein the method comprises the steps of: (col. 2, line 65-col. 3, line 10) providing a base layer(5) on a semiconductor substrate(1) (Fig. 2, col. 3, line 60); depositing a dielectric layer(7) in weakly doped or undoped fashion on the base layer (Fig. 3, col. 4, lines 11-16); applying an implantation mask (13) and patterning in such a way that an opening remains in a region provided for a later extrinsic base (Fig. 7, col. 4, lines 41-43); introducing a dopant of a first conductivity type into the dielectric layer after the application of the mask; using

$BF_2$ as the dopant; indifussing, in a controlled thermal step, the dopant into the semiconductor substrate from the dielectric layer, an extrinsic base doped in low-resistance fashion arising (Fig. 5, col. 4, lines 25-34).

Regarding claim **17**, Johansson et al. discloses a method in which an oxide layer is deposited as the dielectric layer(5) (DS) (col. 4, lines 11-14).

Regarding claim **18**, Johansson et al. discloses a method in which an emitter window(15) is opened in the dielectric layer(5) (Fig. 7, col. 4, lines 41-43).

Regarding claim **19**, Johansson et al. discloses a method in which before the dopant is introduced into the dielectric layer, the emitter is produced by application and patterning of a polycrystalline emitter layer doped with a dopant of the second conductivity type above the emitter window (col. 5, lines 2-15).

Regarding claim **20**, Johansson et al. discloses a method in which the emitter layer is patterned by means of a photopatterned resist mask(13) that remains on the emitter and is later used as an implantation mask for the implantation of the dopant into the dielectric layer(5) (Fig. 8, col. 4, lines 41-59).

Regarding claim **21**, Johansson et al. discloses a method in which, for the production of the semiconductor substrate(1), in a semiconductor wafer doped with a dopant of the second conductivity type, active transistor regions are defined and are electrically insulated by oxide regions; and (Fig. 1, col. 3, lines 47-56) in which a base layer weakly doped with a dopant of the first conductivity type is grown epitaxially over the whole area (Fig. 2, col. 3, lines 60-66).

Regarding claim **23**, Johansson et al. discloses a method in which BF.sub.2 is implanted for the introduction of the dopant into the dielectric layer (Fig. 5, col. 4, lines 25-28).

Regarding claim **24**, Johansson et al. discloses a method in which $BF_2$ can be indiffused into the dielectric layer from the gas phase (Fig. 5, col. 4, lines 25-29).

Regarding claim **26**, Johansson et al. discloses a method in which the dielectric layer is removed after the patterning of the emitter layer and after the outdiffusion of the dopant in uncovered regions by etching (col. 5, lines 11-14).

Regarding claim **28**, Johansson et al. discloses a method in which a photomask(13) applied over an oxide layer over the emitter is used as the implantation mask, said photomask already having been used beforehand for the patterning of the emitter layer (Fig. 7, col. 4, lines 41-43).

## *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 22, 25, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johansson et al. (US 6,40,810 B1) in view of Johnson (6,028,345).

Johansson et al. discloses the method substantially as claimed. See the preceding rejection of claims 16-21, 23, 24, 26 and 28 under 35 U.S.C. 102(b).

However, Johansson et al. fails to show that a buried collector layer is doped with a dopant of the second conductivity type, the doping of the emitter layer, and the production of metallic contacts.

Regarding claim **22**, Johnson discloses a method in which a buried collector layer(102) doped with a dopant of the second conductivity type is produced by implantation in the semiconductor wafer in the active transistor region(100), said collector layer serving for electrical connection of the collector (Fig. 3, col. 3, lines 40-46).

Regarding claim **25**, Johnson discloses a method in which the emitter layer is doped with arsenic, in which, during the indiffusion of the dopant into the base layer (BS)(110), arsenic also indiffuses into a surface region of the base layer (BS) from the emitter (E)(130) (Fig. 4, col. 3, line 63-col. 4, line 7).

Regarding claim **27**, Johansson et al. discloses a method further comprising the steps of: providing an n-doped semiconductor (Fig. 1, col. 3, lines 47-53); growing a p-doped base layer(5) epitaxially on the semiconductor wafer(1) over the whole area (Fig. 2, col. 3, lines 60-64); applying a dielectric layer(7) in weakly doped or undoped fashion on the base layer; opening an emitter window(15) in the dielectric layer (col. 4, lines 11-14); producing the emitter by application and patterning of an As-doped polycrystalline emitter layer above the emitter window (Fig. 9, col. 4, lines 53-59, 64-65); introducing $BF_2$ as the dopant into the dielectric layer with the aid of an implantation mask (Fig. 5, col. 4, lines 25-28).

Johnson discloses method in which in a controlled thermal step, indiffusing boron from the dielectric layer into the base layer in the region of the extrinsic base, the latter acquiring low

resistance, and simultaneously indiffusing arsenic into an upper region of the base layer from the emitter through the emitter window (Fig. 4, col. 3, line 47-col. 4, line 7).

Regarding claim **29**, Johnson et al. discloses a method in which the collector connection is effected via an $n^+$-doped buried layer, and in which, over the emitter and in the region of the extrinsic base, the respective semiconductor is uncovered and metallic contacts(150) are produced above the latter (Fig. 8a-d, col. 4, lines 22-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Johnson with the method of Johansson et al. to form a bipolar transistor that includes a collector region comprising a buried collector and doped epitaxial layer (col. 2, lines 53-61).

## ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENISHA V. FORD whose telephone number is (571)270-3328. The examiner can normally be reached on Monday-Thursday 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Walter L. Lindsay, Jr./
Primary Examiner, Art Unit 2812

KVF